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Single-Phase Dual-Mode Interleaved Multi-level Inverter (DMIMI) for PV Applications

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***Abstract*— A novel single-phase transformerless dual-mode interleaved multi-level inverter (DMIMI) is proposed, which can inject a highly sinusoidal AC current to the grid even with the input DC voltage less than the peak grid voltage. Furthermore, dead-beat controllers are developed to directly calculate the optimal duty cycles in a digital control platform. As compared to the traditional dual-mode multilevel approaches, the DMIMI offers a high efficiency, less number of components conducting simultaneously in each operation mode and the capability of reactive power exchange. The paper presents the theoretical analysis and the experimental results obtained from a 1 kW prototype. The experimental results reveal that the proposed DMIMI can achieve a high conversion efficiency and a low leakage current as well as a high quality grid current.**

***Index Terms*—Dual-mode time-sharing, interleaved, leakage current, multi-level inverter, transformerless.**

I. Introduction

TRANSFORMERLESS PV inverters have already found both technical and commercial acceptance due to their advantageous characteristics like high efficiency, low cost and small size [1]–[3]. The generated voltage by the PV panels may be less than the minimum required DC voltage for the proper operation of the inverter circuit, which requires a boost converter to step up the PV voltage to the minimum required level [4], [5]. The main drawback of these topologies is that the power semiconductors of the boost stage are switching at high frequency during the whole period of the AC voltage waveform. Consequently, the converter efficiency decreases [6].

In order to avoid unnecessary losses of the conventional two-stage transformerless PV inverters, many dual-mode time sharing techniques are proposed. In this way, only when the PV voltage is below the instantaneous grid voltage value, the boost stage is activated. Several different topologies and control algorithms of these high-efficient converters are already available in literature [7]–[13]. As a most recent achievement, it is proposed that the DC-to-DC boost converter connects in parallel, instead of in cascade, with the main inverter stage [13], [14]. Therefore, only a fraction of the PV power is processed by the step-up converter even at low PV voltages. These converters are shown in Fig. 1. Clearly, when the step-up stage is active, the upper capacitor is charged through the DC inductor, resulting in a total DC voltage across both capacitors to be above the peak AC voltage. This configuration lets multi-level operation of the inverter stage that itself offers decreased voltage stress on semiconductors and higher output current quality.

A main concern with the transformerless PV inverters is the leakage current, which may result in serious technical and safety problems. The conventional inverter circuits cannot anymore address the rigid requirements of the standards, such as VDE 0126-1-1 [15], regarding the maximum tolerable leakage current. The inverter stage of Fig. 1(a) utilizes the AC decoupling technique by turning on the switches S_5 and S_6 during the freewheeling operation modes, like the conventional HERIC [16] and the inverter stage of Fig. 1(b) uses the double grounding decoupling technique by turning on the switches S_3 and S_4 during the freewheeling operation modes, which was originally employed in [17]–[19].

While the ideas of [13] and [14] are very interesting, both converters suffer from some major drawbacks. First, the step-up chopper in both converters operates in the continuous conduction mode (CCM) to limit the peak current of the semiconductors and the step-up inductor. So, as already

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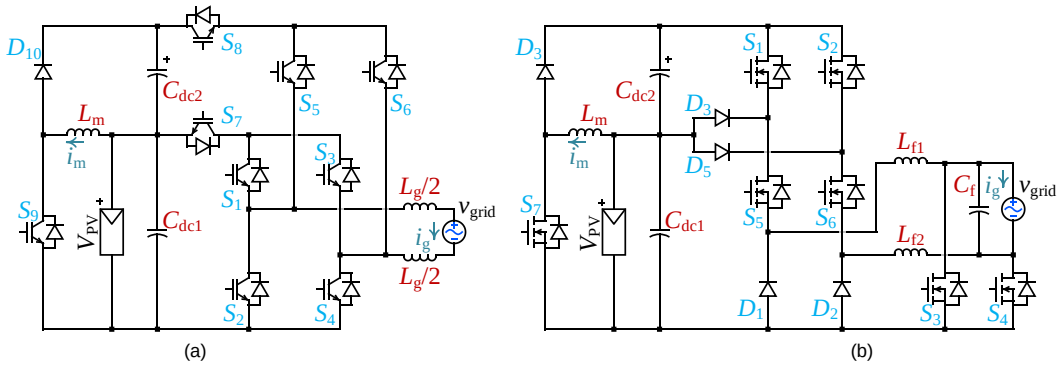

Fig. 1. Multi-level inverters with parallel integrated step-up chopper proposed in: (a) [13] and (b) [14].

expected with any step-up chopper circuit, the high reverse recovery current of the step-up diode causes losses and short circuits of the DC side capacitors. Even in the CCM mode, the high peak current through the step-up inductor and the semiconductors limit the power level of the converter circuit. Another drawback with the converter of [14] is that the high frequency switch of the step-up stage is always active that considerably reduces the efficiency. At the inverter side of both circuits, the problem of leakage current is still a real concern. Specially the converter of [13] cannot conform to the standards without added common mode filters. Therefore, at the cost of increased size and volume and reduced efficiency, the common mode filter inductors are employed. The main reason for this problem with the converter of [13] is that the common mode voltage contains the switching frequency components at all operation modes of the converter. More comparative performance details will be presented later. On the other hand, both inverters have a high number of semiconductors, which calls for a wise control and modulation technique to minimize the number of semiconductors simultaneously in the current path as well as the number of commutations. However, both converters of [13] and [14] could not be very successful in this regard.

In order to extract the maximum benefits out of the ideas already presented in [13] and [14], an improved circuit is proposed in this paper.

At the DC side, a two-phase interleaved parallel step-up chopper is employed; therefore, the current stresses of the semiconductors and the DC side inductors are significantly reduced. Besides improving the efficiency, the interleaved configuration allows the converter to work in the discontinuous conduction mode (DCM). Hence, the reverse recovery current problem of the diodes is solved, also a zero-current switching (ZCS) for the step-up switches is achieved that significantly reduces the losses, switching transients and electromagnetic interferences. As [13] and [14], the proposed converter can also operate with a wide range of PV voltage variations; however, on contrary to [14], the step-up stage is active only when it is necessary.

Also, the high frequency component of the common mode voltage is limited, therefore the RMS value of leakage current is below the standard limits. With the proposed modulation technique, the total number of semiconductors conducting simultaneously is minimized, which again improves the overall converter efficiency.

Furthermore, it must be mentioned that, the reactive power support has already become a necessary feature in many standards and grid codes, such as VDE-AR-N-4105. According to [20], to have the reactive power capability, a PV inverter needs to provide a current path during the zero-voltage states at the negative power region (NPR). The NPR is defined as the time region during which the instantaneous values of the grid current and voltage have opposite polarities.

A modified version of modulation strategies already proposed for H5, H6 and HERIC in [20], [21] and [22] developed for the proposed inverter that also lets the reactive power exchange capability.

Finally, two dead-beat controllers, one for the voltage control of the step-up chopper and another for the current control of the inverter are adopted that offer accurate, fast and smooth control performance under different working conditions.

The paper is organized as follows. The operation modes, the modulation strategy and the components design of the proposed converter are presented in section II. Then, the control algorithms are explained in details in section III. Finally, the experimental results in section IV are presented followed by the conclusion in section V.

II. Proposed DMIMI for PV Applications

A. Operation modes of DMIMI

The circuit diagram of the proposed dual-mode interleaved multi-level inverter (DMIMI) is presented in Fig. 2. Clearly, a two-phase interleaved step-up chopper is connected in parallel with a novel step-down inverter. According to the instantaneous value of the grid and the DC source voltages, this converter works in two different modes of operation, i.e. step-down 3-level and step-up 3-level modes. The proposed DMIMI consists of ten power switches S_{m1}, S_{m2}, S_1-S_8, four diodes D_{m1}, D_{m2}, D_1 and D_2 and passive elements as the grid filter inductor, L_g, two DC side inductors, L_{m1} and L_{m2}, DC side capacitor C_{dc1} and two DC-link capacitors C_{dc2} and C_{dc3}.

As shown in Fig. 3, during the time when the magnitude of the PV voltage is higher than the absolute instantaneous voltage of the grid, the step-up stage is inactive and the simple 3-level operation mode of the converter is activated. Consequently, three levels are produced in the output of the inverter (V_{AB} = 0 and ± V_{PV}).

When the PV voltage is less than the grid voltage, then the step-up 3-level mode of the converter is initiated. The interleaved step-up chopper is active now and again three levels are generated at the output port (V_{AB} = 0 and ± (V_{PV} + V_{dc1})).

The main task of the parallel DC chopper is charging the C_{dc1} through the inductor L_{mk} and diode D_{mk}, which is complementary commutates with S_{mk}, kϵ{1,2}.

While S_{mk} is on, the inductor L_{mk} is charged through the PV

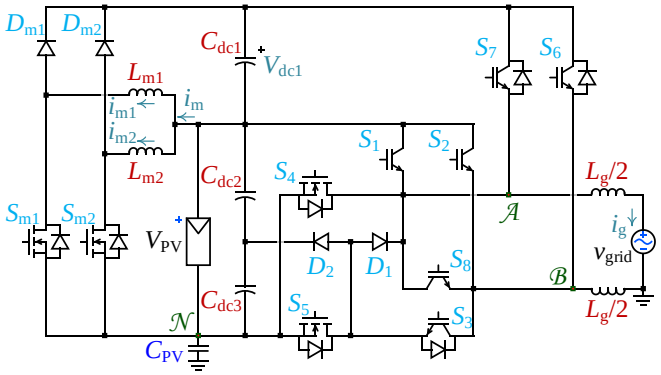

Fig. 2. Proposed DMIMI.

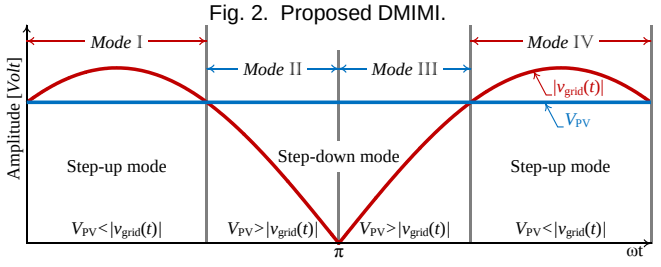

Fig. 3. Operation modes of DMIMI assuming PF = 1.

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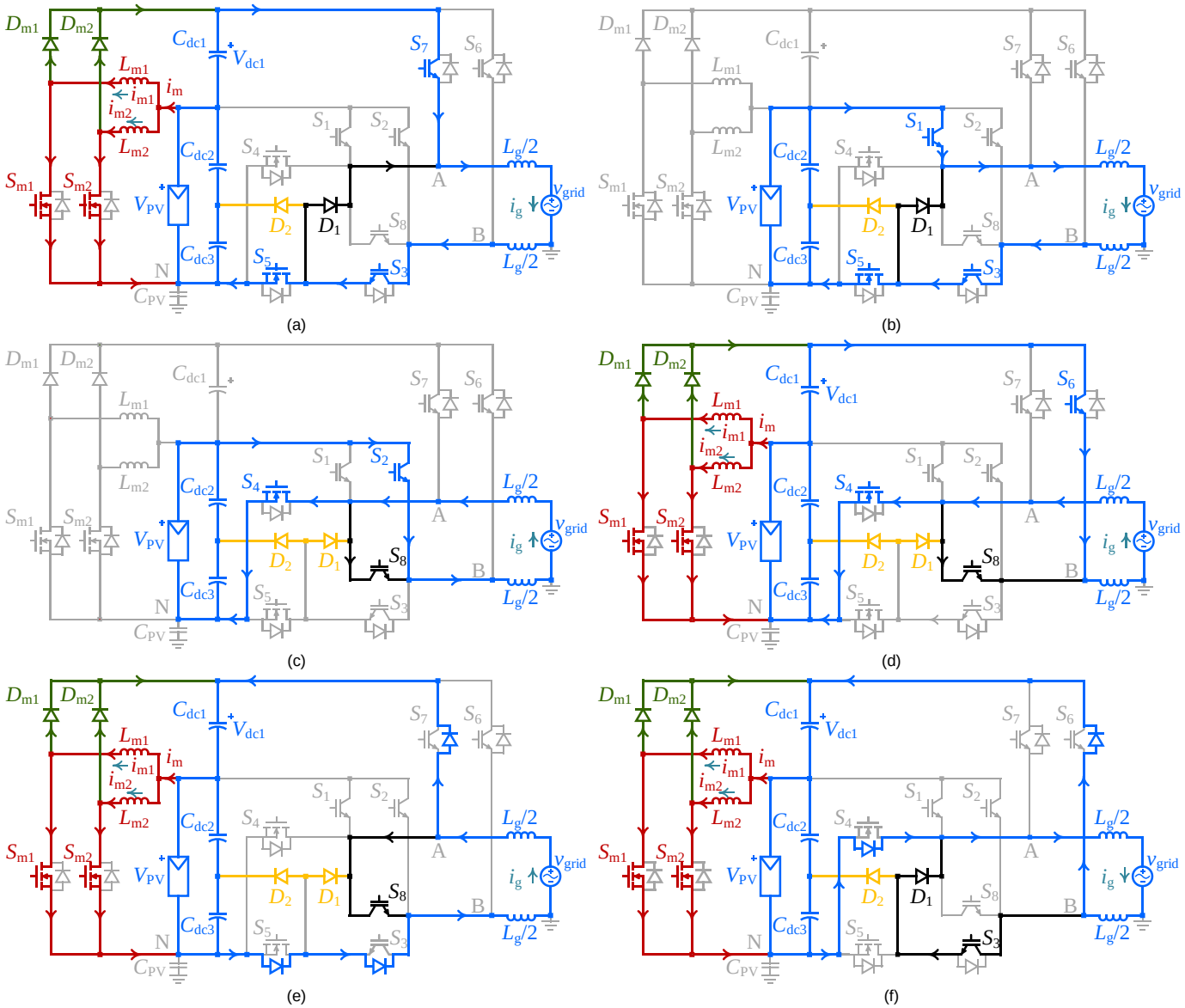

Fig. 4. Modes of operation: (a) I, (b) II, (c) III, (d) IV, (e) V and (f) VI (blue line: inverter mode, black line: zero state mode, red line: DC chopper charging mode, green line: DC chopper discharging mode and yellow line: passive clamping mode).

panels and its current increases. When S_{mk} is turned off, the stored energy in the inductor is transferred to the output capacitor C_{dc1}, which is large enough to consider its voltage almost unchanged.

Clearly, the reverse recovery of diode D_{mk} can cause a severe shoot-through of the three in series connected capacitors, C_{dc1}, C_{dc2} and C_{dc3}. The large reverse recovery current, especially at high powers, causes EMI problems and can readily damage the converter. To avoid this problem, the value of L_{m1} is designed such that the DC chopper works in the DCM mode. When D_{mk} is fully off and the current through it is zero, then S_{mk} is turned on. Hence, the reverse recovery current of diode is blocked. In DCM operation, the current stresses of the active and passive devices are higher than the CCM operation. So, the DC chopper is interleaved with two phases. In this way, not only the current stresses of the elements are reduced, but also the ripple frequency at the output of the DC chopper is twice the switching frequency and thereby a smaller C_{dc1} is required. In addition, the DC side power switches are turned on at the zero current, therefore the switching transients and power losses are reduced significantly.

At the inverter side, the major concerns are the efficiency, ratings of semiconductors and more importantly the leakage current. As can be seen later, during the simple unipolar operation, the inverter can successfully maintain the common mode voltage constant and during the multi-level operation, the DC source is decoupled from the grid during the freewheeling periods. Consequently, a low level of leakage current is ensured.

The proposed DMIMI works in six distinct modes of operation (modes *I* to *IV* for PF = 1 and modes *V* and *VI* for PF ≠ 1), depicted in Figs. 3 and 4, and illustrated below:

Mode I: In the step-up 3-level mode and during the positive half cycle of the grid voltage waveform, the voltage across the C_{dc1} is maintained by adjusting the duty cycle of the interleaved DC chopper. Both S_{m1} and S_{m2} are PWM controlled with the switching frequency (f_{sw}) and 180° phase-shift in the carrier waveforms. The diode D_{mk} immediately after turning off the switch S_{mk} conducts as demonstrated in Fig. 4(a). Its current decays to zero before the start of the next switching

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period. At the inverter side, the switch S_3 is always on and S_5 and S_7 are together turned on and off (PWM controlled) to generate the voltage levels $V_{AB} = V_{PV} + V_{dc1}$ and $V_{AB} = 0$, respectively. Clearly, the grid is decoupled from the PV during the freewheeling (when $V_{AB} = 0$). The grid current path is through D_1 and S_3 as shown in Fig. 4(a).

Mode II: When the instantaneous grid voltage is less than the PV voltage, the step-up operation is no longer necessary. The switches S_1 and S_5 are now PWM controlled and the whole energy is transferred from only the PV panels to the grid and the PV voltage appears at the output of the inverter ($V_{AB} = V_{PV}$), whilst S_3 is still kept on as shown in Fig. 4(b). When S_1 and S_5 are turned off, then D_1 automatically starts conducting and the zero voltage level is generated ($V_{AB} = 0$). The freewheeling action is the same as before.

Mode III: During the negative half cycle, the switch S_8 is always on (instead of S_3). As the mode II, the inverter voltage changes between -V_{PV} and 0. As Fig. 4(c) depicts, S_2 and S_4 are PWM controlled together. The zero-voltage level is automatically generated when the high frequency switches are turned off. The freewheeling path is also created through the switch S_8, meanwhile only one semiconductor device is conducting during the freewheeling.

Mode IV: As indicated in Fig. 4(d), in the step-up 3-level mode operation and when the grid voltage goes in to the negative half cycle, the interleaved DC chopper is activated again in order to maintain the voltage of C_{dc1}. The Switches S_4 and S_6 are also turned on and off together with the PWM signal. The freewheeling is exactly the same as mode III.

Finally, the DC link capacitors of the PV panels are split and the diode D_2 is added to the middle point of the DC capacitors as already proposed for conventional H5 inverter in [3] as a simple and effective technique to suppress the high-frequency contents of the common-mode voltage and consequently reduce the leakage current even more effective.

The switches S_1 and S_2 must block the reverse current, otherwise the capacitor C_{dc1} will become shorted during the operation of S_6 and S_7. Also, S_3 and S_8 need to block the reverse current.

This converter utilizes a simple PWM modulation strategy, shown in Fig. 5(a). In this figure, m and d are the modulation index of the inverter stage and the duty cycle of the chopper circuit, respectively, which are set by the grid current and the C_{dc1} voltage controllers, respectively. These controllers will be explained in section III.

Fig. 5(c) shows the realization of the overall modulation algorithm, which is also capable of reactive power exchange. The two extra modes of operation during the NPRs are shown in Fig. 5(b) and explained below:

Mode V: During the negative half cycle of the grid voltage and when the instantaneous value of i_g is positive (refer to Fig. 4(e)), the current through L_g increases in the freewheeling circuit consisting of S_3 and D_1 and the anti-parallel diodes of S_4 and S_6.

Mode VI: During the positive half cycle of the grid voltage and when i_g is negative (refer to Fig. 4(f)), the current through L_g increases in the freewheeling circuit composed of S_8 and the anti-parallel diodes of S_3, S_5 and S_7.

B. Component Design

The total DC link capacitor C_{DC} (C_{dc2} in series with C_{dc3}) is a buffer for the instantaneous power difference between the grid and the PV. Thus, to maintain the ripple of the DC-link voltage (ΔV_{DC}) below a specific value, C_{DC} must satisfy the following equation [23]

$$C_{DC} \geq \frac{P_{out}}{\omega_0 V_{PV} \Delta V_{DC}} \quad (1)$$

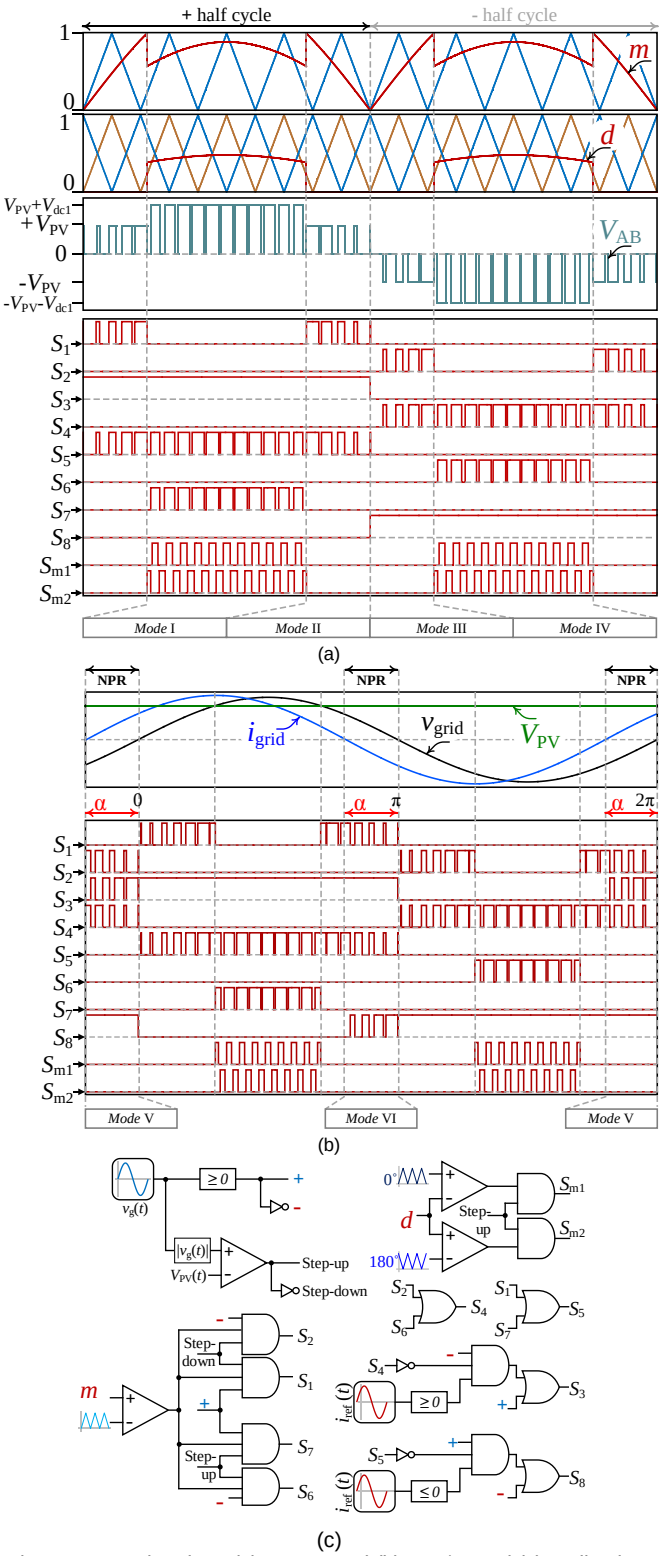


Fig. 5. PWM signals at (a) PF = 1 and (b) PF ≠ 1 and (c) realization.

where P_{out} is the average output power, ω_0 is the grid angular frequency and V_{PV} is the PV voltage.

The value of grid side filter inductor, L_g, is chosen from the maximum allowed current ripple, Δi_g, as follows [24]

$$L_g \geq \frac{(V_{DCx} - v_g)v_g}{2\Delta i_g \times V_{DCx}} T_s \tag{2}$$

where $v_g = 220\sqrt{2}\sin(\omega_0 t)$ is the grid voltage, V_{DCx} is V_{PV} and $V_{PV} + V_{dc1}$ during the step-down and the step-up modes of operation, respectively, T_s is the sampling time period and Δi_g is the maximum permissible ripple of the grid injected current which is given 5% of the rated current. The value of L_g can be selected from (2) as 2 mH.

To ensure that the DC chopper works in the DCM operation mode, equation (3) must be satisfied:

$$I_{mk,min} = \frac{P_{out}(V_{PV} + V_{dc1})}{4V_{PV}V_{dc1}} - \frac{V_{PV}V_{dc1}}{(V_{PV} + V_{dc1})L_{mk}} T_s < 0 \tag{3}$$

that can be rearranged for the required inductance as

$$L_{mk} < \frac{4(V_{PV}V_{dc1})^2}{P_{out}(V_{PV} + V_{dc1})^2} T_s . \tag{4}$$

To keep the output voltage ripple of V_{dc1}, (Δv_{dc1}) below a certain value, the capacitor C_{dc1} must satisfy

$$C_{dc1} \geq \frac{\Delta Q_{Cdc1}}{\Delta v_{dc1}} \tag{5}$$

where ΔQ_{Cdc1} is the overall charge change of the capacitor that can be readily calculated as the integration of its current waveform during a sampling period as

$$\Delta Q_{Cdc1} = \frac{V_{PV}V_{dc1}}{8(V_{PV} + V_{dc,1})L_{mk}} T_s^2 . \tag{6}$$

The value of V_{dc1} is chosen such that the total voltage (V_{dc1} + V_{PV}) is enough higher than the peak grid voltage, e.g. 350 V_{DC} for the 220 V_{AC} grid. Therefore $V_{dc1} = 350 - V_{PV}$.

TABLE I
COMMON MODE AND POLE VOLTAGES

	V_{AN}	V_{BN}	V_{CM}
Mode I	$S_7(V_{PV} + V_{dc1}) + \bar{S}_7 \frac{V_{PV}}{2}$	$\bar{S}_7 \frac{V_{PV}}{2}$	$\frac{V_{PV} + S_7 V_{dc1}}{2}$
Mode II	$S_1 V_{PV} + \bar{S}_1 \frac{V_{PV}}{2}$	$\bar{S}_1 \frac{V_{PV}}{2}$	$\frac{V_{PV}}{2}$
Mode III	$\bar{S}_2 \frac{V_{PV}}{2}$	$S_2 V_{PV} + \bar{S}_1 \frac{V_{PV}}{2}$	$\frac{V_{PV}}{2}$
Mode IV	$\bar{S}_6 \frac{V_{PV}}{2}$	$S_6(V_{PV} + V_{dc1}) + \bar{S}_6 \frac{V_{PV}}{2}$	$\frac{V_{PV} + S_6 V_{dc1}}{2}$

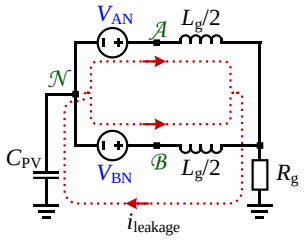


Fig. 6. Simplified common mode model of DMIMI.

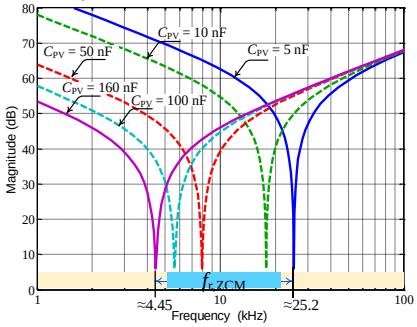


Fig. 7. Magnitude Bode plot of Z_{CM}.

C. Common Mode Analysis

The simple equivalent common mode circuit is shown in Fig. 6, which includes the stray capacitor between the ground and the PV array, C_{PV}, the ground resistance, R_g, the filter inductance, L_g and the pole voltages. The leakage current, $i_{leakage}$, originated from the common mode voltage (V_{CM}) can be written as [3]

$$i_{leakage} = \frac{V_{CM}}{Z_{CM}} = \frac{(V_{AN} + V_{BN})/2}{0.25L_g s + R_g + 1/(C_{PV} s)} \tag{7}$$

where Z_{CM} is the common mode impedance that its magnitude is near infinity and minimum at the origin and its resonance frequency, $f_{r,ZCM}$, respectively.

The pole and common mode voltages are summarized for different modes in Table I, from which it can be concluded that the leakage current is almost negligible during the converter operation in modes II and III. Contrary, the high frequency operation of S_7 and S_6 in modes I and IV causes that V_{CM} varies at the switching frequency (f_{sw}) and the leakage current may become large if the common mode impedance is small at f_{sw}. To avoid this situation, $f_{r,ZCM}$ must be much less than f_{sw} (the frequency of variations of V_{CM}).

Considering, the magnitude Bode plot of Z_{CM} as shown in Fig. 7, $f_{r,ZCM}$ must be much below the first switching sideband of V_{CM} to avoid any excessive $i_{leakage}$. Otherwise, the high-amplitude switching harmonics over the low-amplitude impedance at the resonance frequency results in a high value of leakage current around that frequency.

In this work, f_{sw} is chosen as 30 kHz, which is much higher than the possible range of $f_{r,ZCM}$. Therefore, as it will be shown later, the value of $i_{leakage}$ is well below to the standard limits.

D. Power loss analysis

The total power loss of the proposed converter, P_T, is calculated for each mode by summing the power losses of the components comprising the power section and the output filter. The power loss equations are summarized in Table II.

TABLE II
POWER LOSS EQUATIONS.

Total power loss	$P_T = P_{con} + P_{sw} + P_L$
Conduction loss	$P_{con} = \sum_i \frac{1}{T} \int_t^{t+T} \left[v_{0,Si} i_{Si}(t) + r_{0,Si} i_{Si}^2(t) \right] dt$
Switch loss	$P_{sw,Si} = \frac{f_{sw}}{2} \sum_i \frac{1}{T} \int_t^{t+T} v_{Si}(t) i_{Si}(t)(t_{r,Si} + t_{f,Si}) dt$
Diode loss	$P_{sw,Di} = \frac{f_{sw} I_{rr} t_b}{4} \sum_i \frac{1}{T} \int_t^{t+T} v_{Di}(t) dt$
Inductor loss	$P_L = r_{Lm} I_{Lm}^2 + r_{Lg} I_g^2 + 2(k f_{sw}^{\alpha} B^{\beta} \times W \times 10^{-3})$

In this table, P_{con} and P_{sw} are the conduction and switching losses, respectively, of power semiconductors and P_L is the core and winding losses of the inductors occurring in L_{mk} and L_g.

i_{Si} is the current conducted by the semiconductor power devices and $v_{0,Si}$ and $r_{0,Si}$ are the voltage drop and the on-state resistance of the power devices, respectively.

v_{Si} is the voltage blocked by the semiconductors and t_r and t_f are the rise-time and the fall-time of them.

$I_{rr} = 2Q_{rr} / t_{rr}$, and $t_{rr} = t_a + t_b$, which can be replaced from the datasheet. k is the eddy current loss coefficient, B is the magnetic flux variation, α and β are constants that depend on the core type and W is the core weight in grams. Kool-Mμ core is employed for both inductors (k = 0.000693, α = 1.460, β = 2.0 and W = 570 g).

The power-loss calculation of the proposed converter is presented in results section. It can be seen that the ZCS and the interleaved operation of the DC chopper offer a low switching loss for the DMIMI. These results are later confirmed through experiments.

III. Control Design

As mentioned before, the control of the proposed converter includes two algorithms: one to maintain V_{dc1} (voltage controller) and the other to shape the grid current at the inverter stage (current controller). The overall control system is shown in Fig. 8. By comparing the instantaneous grid voltage and the PV voltage, either step-down or step-up mode of operation is first determined.

In this work a simple yet efficient digital control concept, called dead-beat (DB), is adopted for both voltage and current controllers. As will be shown, the DB voltage controller only requires the value of C_{dc1} to directly calculate the duty cycle, d, of the chopper from the measured and reference V_{dc1} and measured inductor and grid currents. The DB current controller can also simply determine the modulation index, m, for the inverter stage directly from the measured grid voltage, measured and reference grid current and the measured DC voltage with the grid inductance value as the only parameter to be known.

A. Voltage control

As shown in Fig. 9(a), in step-up operation mode, when the

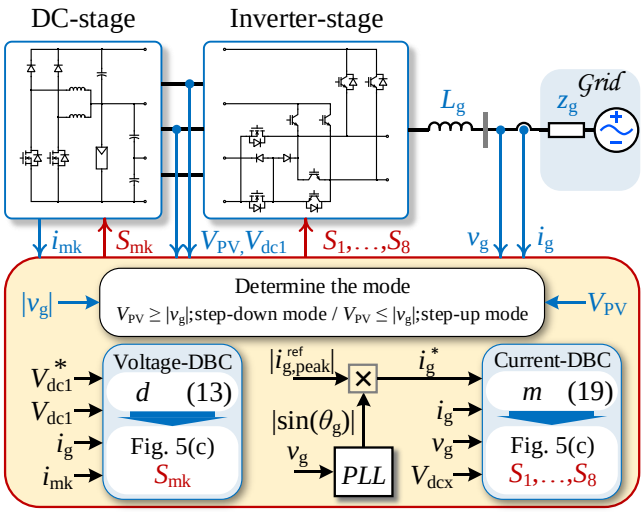
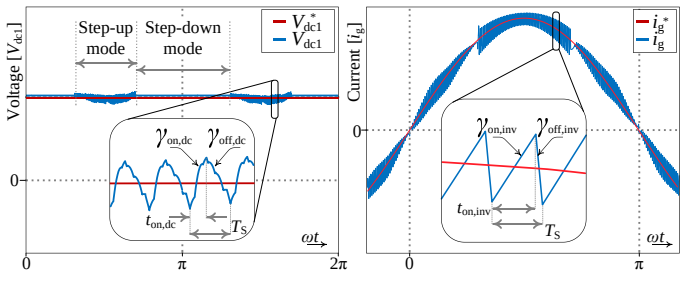


Fig. 8. Control diagram of proposed DMIMI.



(a) (b)

Fig. 9. (a) V_{dc1} and (b) i_g variations during each operation mode.

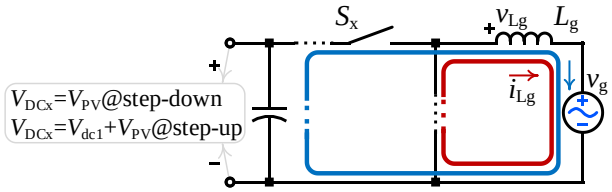


Fig. 10. Simple equivalent circuit of the inverter stage during conduction of S_x (blue line) and freewheeling (red line).

chopper is active, while S_{mk} is on, the current through C_{dc1} can be determined as

$$i_{Cdc1} = C_{dc1}\frac{dV_{dc1}}{dt} = -i_g \,. \tag{8}$$

Similarly, when the switch S_{mk} is off, the capacitor current is

$$i_{Cdc1} = C_{dc1}\frac{dV_{dc1}}{dt} = i_{mk} - i_g \tag{9}$$

The slope of the capacitor voltage during S_{mk} on state ($\gamma_{on,dc}$) and during S_{mk} off state ($\gamma_{off,dc}$) can be determined as

$$\begin{cases} \gamma_{on,dc} = \dfrac{dV_{dc1}}{dt} = \dfrac{-i_g}{C_{dc1}} \\ \gamma_{off,dc} = \dfrac{dV_{dc1}}{dt} = \dfrac{i_{mk} - i_g}{C_{dc1}} \end{cases} \tag{10}$$

Now one can predict the capacitor voltage at the next sampling period ($V_{dc1}[n+1]$) from its current value ($V_{dc1}[n]$), by using the slopes already determined in (10) for the step-up mode of operation, i.e.

$$V_{dc1}[n+1] = V_{dc1}[n] + \gamma_{on,dc}t_{on,dc} + \gamma_{off,dc}t_{off,dc} \tag{11}$$

where $t_{on,dc}$ and $t_{off,dc}$ are the S_{mk} on and off state dwell times, respectively during the step-up operation.

The controller is intended to eliminate the error, v_e, between the reference voltage (V_{dc1}^*) and $V_{dc1}[n+1]$, i.e.

$$v_e = V_{dc1}^* - V_{dc1}[n+1] = V_{dc1}^* - V_{dc1}[n] - \gamma_{on,DC}t_{on,DC} - \gamma_{off,DC}t_{off,DC} = 0 \tag{12}$$

Then, $t_{on,dc}$ and consequently the optimal duty cycle can be determined as

$$d = \frac{t_{on,dc}}{T_s} = \frac{C_{dc1}(V_{dc1}^* - V_{dc1}[n]) - (i_{mk}[n] - i_g[n])T_s}{(2i_g[n] - i_{mk}[n])T_s} \,. \tag{13}$$

B. Current control

The current controller is aimed to shape the current through L_g, shown as i_g, as a pure sinusoid, which is in phase with the grid voltage. As shown in Fig. 9(b) a simple DB current controller is again developed for this goal. The simple equivalent circuit of the inverter stage is shown in Fig. 10. In

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the equivalent circuit, when S_x is on, the voltage across L_g can be determined as

$$v_{Lg} = L_g \frac{di_g}{dt} = V_{DCx} - v_g \tag{14}$$

where V_{DCx} is V_{PV} and $V_{PV} + V_{dc1}$ during the step-down (modes II and III) and the step-up (modes I and IV) operations, respectively. When the equivalent switch S_x is off, then the inductor voltage is

$$v_{Lg} = L_g \frac{di_g}{dt} = -v_g . \tag{15}$$

The slope of the inductor current during S_x on state ($\gamma_{on,inv}$) and off state ($\gamma_{off,inv}$) can be written as

$$\begin{cases} \gamma_{on,inv} = \dfrac{di_g}{dt} = \dfrac{V_{DCx} - v_g}{L_g} \\ \gamma_{off,inv} = \dfrac{di_g}{dt} = \dfrac{-v_g}{L_g} \end{cases} \tag{16}$$

Now one can predict the inductor current at the next sampling period ($i_g[n+1]$) from its current value ($i_g[n]$), by using the slopes already determined in (16), i.e.

$$i_g[n+1] = i_g[n] + \gamma_{on,inv} t_{on,inv} + \gamma_{off,inv} t_{off,inv} \tag{17}$$

where $t_{on,inv}$ and $t_{off,inv}$ are the S_x on and off state dwell times, respectively.

The controller is intended to eliminate the error, i_e, between the reference current (i_g^*) and $i_g[n+1]$, which translates to

$$i_e = i_g^* - i_g[n+1] = i_g^* - i_g[n] - \gamma_{on,inv} t_{on,inv} - \gamma_{off,inv} t_{off,inv} = 0 . \tag{18}$$

Then, $t_{on,inv}$ and consequently the optimal modulation index can be determined as

$$m = \frac{L_g (i_g^* - i_g[n]) + v_g[n] T_s}{V_{DCx}[n] T_s} . \tag{19}$$

IV. Performance Evaluation

The performance of the proposed converter is investigated through extensive experiments on a 1 kW test rig, shown in Fig. 11 with the parameters of Table III. A STMicroelectronics STM32F407 floating point digital signal controller is used to implement the DB control algorithm and realize the PWM signals. Figs. 12 and 13 show the full load steady-state performance. It is clear from Fig. 12 that the excellent performance of the proposed converter in injecting a highly sinusoidal current to a harmonically polluted grid. With a closer look at the current waveforms, one may detect slight distortions at mode transitions from the step-down to the step-up and vice versa in the waveforms of Fig. 12(a). However, the THD is slightly higher at the simple unipolar operation mode (2.31%) than the multi-level mode (2.07%). However, both THDs are much below the standard limit of 5%. It must be noted that the grid voltage THD is around 3%. The maximum ripple of the inductance current is less than 5%, which is in accordance to the design value.

The output voltage is shown in Fig. 13 at the multi-level and the simple unipolar modes of operation. As discussed before, at the multi-level operation, the DMIMI generates 5-level voltages as 0, ± V_{PV} (= ± 200V) and ± V_{PV}± V_{dc1} (= ± 350V). The gating signals are generated according to Fig. 5

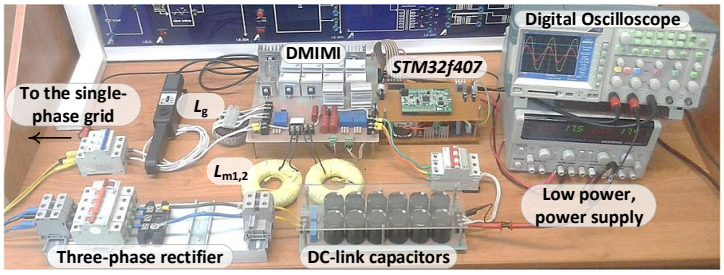


Fig. 11. Experimental hardware prototype.

TABLE III
EXPERIMENTAL SETUP PARAMETERS

Parameter	Value
Input voltage	200 V
Grid voltage	220 V / 50 Hz
Switching frequency	30 kHz
Output power	1 kW
Inductor L_{mk}	0.25 mH
Inductor L_g	2 mH
Capacitor C_{dc1}	23 µF
Capacitor C_{PV}	92 nF
MOSFET	SPW35N60CFD
IGBT	IXGH48N60, IXRH40N120
Diode	IDW16G65C5

and the blocked voltages by semiconductor switches are presented in Fig. 14.

Fig. 15 shows the experimental waveforms of the two-phase interleaved DC chopper currents at full load. Complying with the theoretical analysis, the total output current is the sum of the currents through the interleaved phases and the peak current of each phase is effectively reduced. Also it can be seen that V_{dc1} is regulated with minimum ripples.

The diode and switch current waveforms of Fig. 16 confirm the DCM operation that means D_{mk} is going to the blocking state enough before S_{mk} receives a turn-on gate signal. Therefore the reverse-recovery current of D_{mk} is no longer a problem. Moreover, zero current turn-off of both diode and

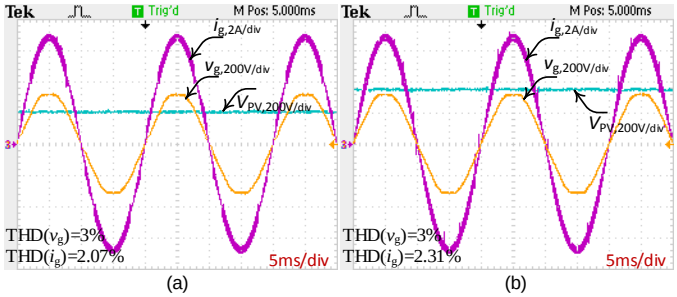


Fig. 12. Waveforms of PV voltage (V_{PV}), grid voltage (v_g), grid current (i_g) for: (a) multi-level operation (V_{PV} = 200 V) and (b) simple unipolar operation (V_{PV} = 350 V).

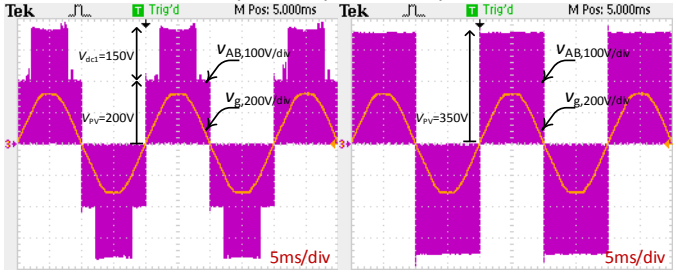


Fig. 13. Waveforms of grid voltage (v_g) and converter voltage (V_{AB}) for: (a) multi-level operation (V_{PV} = 200 V) and (b) simple unipolar operation (V_{PV} = 350 V).

switch reduces the losses and switching transients.

The transient response to step jumps of the DC input voltage and the reference of the grid current are presented in Fig. 17. Obviously a fast current dynamic performance is achieved for both modes. Also a high step change in the PV voltage has almost no effect on the output current waveform.

The DB controllers provide some kind of one-step-ahead prediction that effectively enhances the dynamic performance in response to possible changes and disturbances.

As already mentioned, the leakage current must be concerned with the grid connected PV converters.

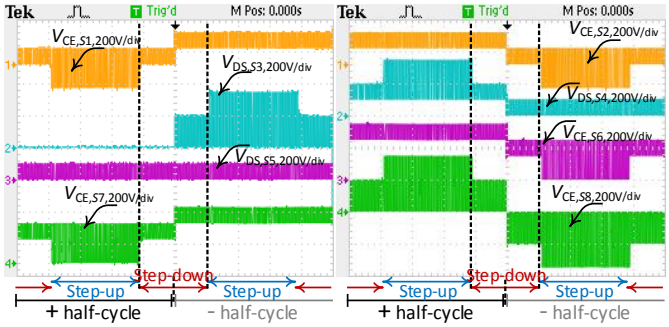


Fig. 14. Collector-emitter voltages of S_1-S_8.

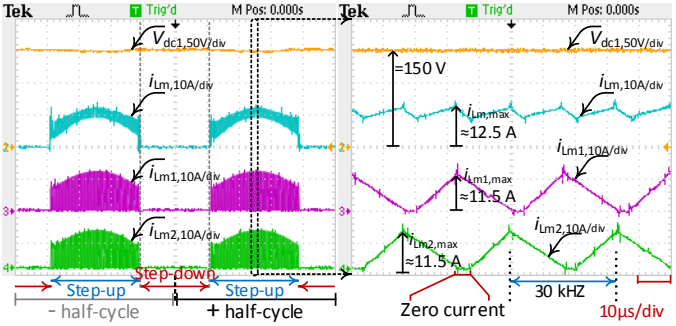


Fig. 15. Waveforms of voltage (V_{dc1}), DC chopper inductor current (i_{Lmk}) and zoomed view for multi-level operation.

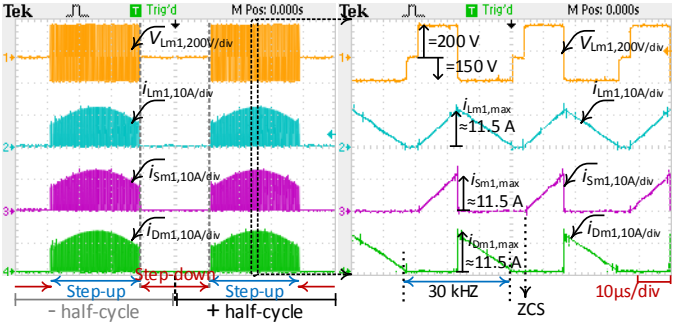
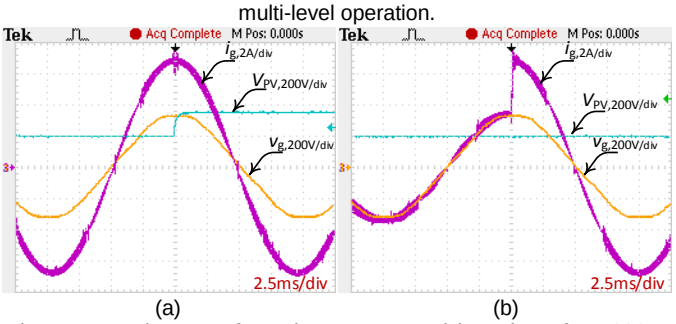


Fig. 16. Waveforms of DC chopper inductor voltage (V_{Lmk}), current (i_{Lmk}), switch current (i_{Smk}), diode current (i_{Dmk}) and zoomed view for multi-level operation.



(a) (b)

Fig. 17. Transient waveforms in response to: (a) V_{PV} jump from 200 V to 350 V and (b) step current jump from half to full-load.

Figs. 18(a) and (b) show the experimental results of the pole voltages, the common mode voltage and the leakage current.

As already expected, the high frequency component of the common mode voltage occurs at around the switching frequency of 30 kHz that lies far outside the possible range of resonance frequency of the common mode impedance. As the result, the RMS value of the grid leakage current is below the standard requirements, for example the limit of 30 mA defined by [15]. Figs. 18(c)-(f) show V_{CM}, V_{AN}, V_{BN} and $i_{leakage}$ for modes I-IV that exactly match the values already calculated from Table I.

As mentioned before, the DB controllers need the values of C_{dc1} and L_g to provide the optimal duty cycles for the DC chopper and the inverter, respectively. Therefore, the performance of the DB controllers, considering the C_{dc1} and L_g mismatches, denoted by ΔC_{dc1} and ΔL_g must be inspected. As an effective measure of control system performance, the THD variations in response to the mismatches is shown in Fig. 19. Firstly the stable operation even with high mismatches is ensured. Secondly the THD of the injected current remains below the requirement of 5% under the full load condition.

As shown in Fig. 20(a) and (b), the proposed PWM strategy operates successfully for both 0.8 leading and 0.8 lagging power factors, which makes the proposed converter a practical and competitive solution in the recent market.

The transient performance of the DMIMI with the proposed PWM strategy is studied experimentally and the results are shown in Fig. 21. It is clear that the proposed modulation technique offers fast and at the same time smooth transitions in response to sudden change of reactive power set-point.

The measured efficiency for different output powers is reported in Fig. 22. For a wide power range from 50 W to 1 kW, the efficiency is above 93% reaching its peak of 97.86% at the output power of 300 W. Furthermore, through the efficiency curve it is possible to calculate the European and CEC weighted efficiencies, as 96.35% and 96.53% for simple unipolar (V_{PV} = 350V) and 96.97% and 97.18% for multi-level (V_{PV} = 200V) modes, respectively.

In order to quantify the interleaved operation, the non-interleaved configuration is simulated with the same inductance, which is employed in the interleaved configuration.

For all four configurations including CCM interleaved/non-interleaved and DCM with ZCS interleaved/non-interleaved, the configuration of inverter side is the same and just the DC side converters are then compared. Therefore, the quantified comparison results among four configurations are summarized in Table IV.

It can be seen that the rating of components and the efficiency of the DCM interleaved configuration is the best.

Finally, a comparison of the proposed transformerless inverter with the well-known competitors is presented in Table V. It must be mentioned that some of the switches (S_1, S_2 and S_3) are unidirectional. Therefore no reactive power can be handled. Although the proposed converter has a higher number of switches and diodes than the topologies of [11], [13] and [14], the number of semiconductors that conduct

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simultaneously is minimum among all. Also, the DMIMI takes advantage of the ZCS operation during the step-up mode, contrary to other competitors in Table V, which highly reduces the switching losses during this operation mode. Consequently, the DMIMI achieves a high efficiency as other successful schemes while it offers additional advantages like a reduced number of active and passive elements conducting simultaneously and a low leakage current. Therefore, it can be considered as a superior candidate for any PV applications.

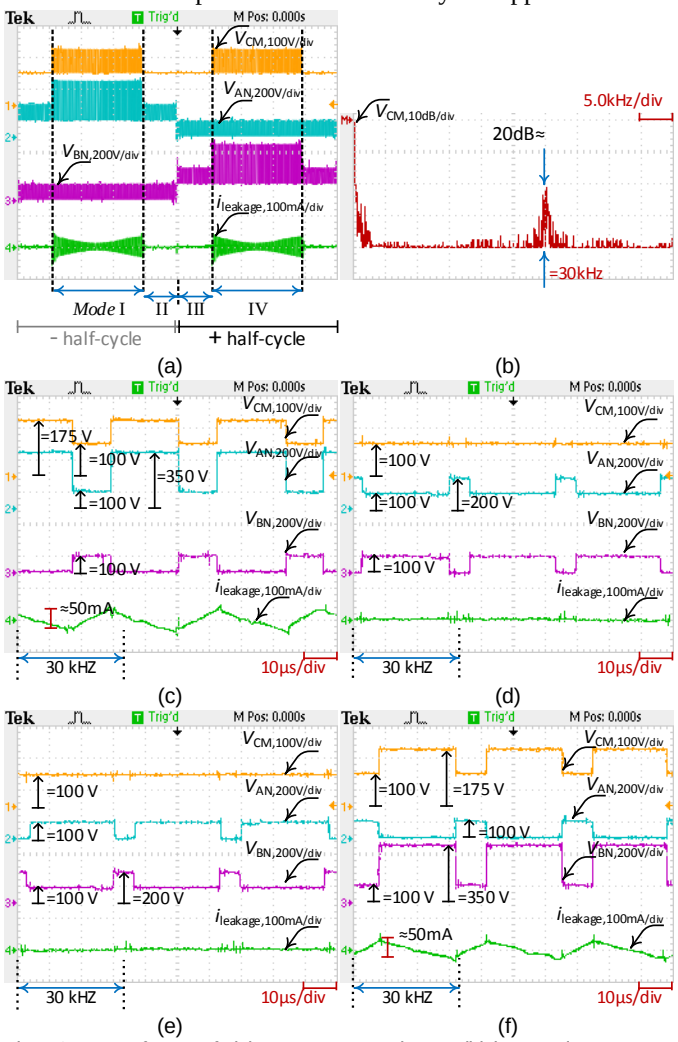

Fig. 18. Waveforms of: (a) V_{CM}, V_{AN}, V_{BN}, $i_{leakage}$, (b) harmonic spectrum of V_{CM}, and zoomed view of waveforms at (c) mode I, (d) mode II, (e) mode III and (f) mode IV.

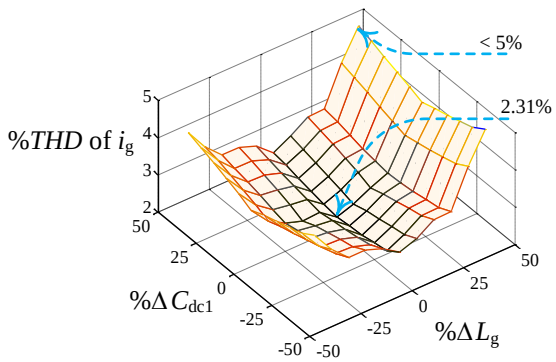

Fig. 19. Grid-injected current %THD versus C_{dc1} and L_g mismatches under nominal power, THD is always below 5% with the maximum and minimum of 4.7% and 2.31%, respectively.

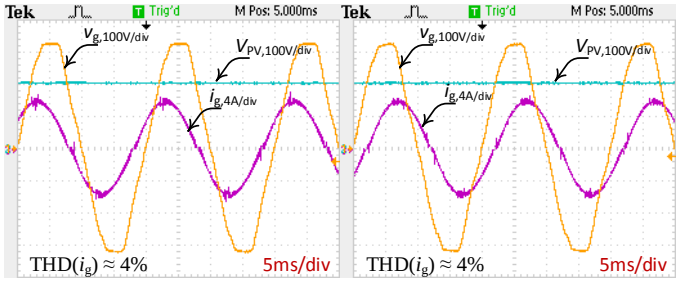

Fig. 20. Waveforms of PV voltage (V_{PV}), grid voltage (v_g), grid current (i_g) under: (a) 0.8 leading and (b) 0.8 lagging power factors.

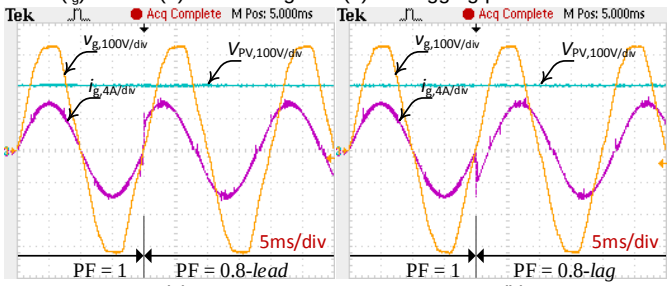

Fig. 21. Transient waveforms from unity to (a) 0.8 leading and (b) 0.8 lagging power factors.

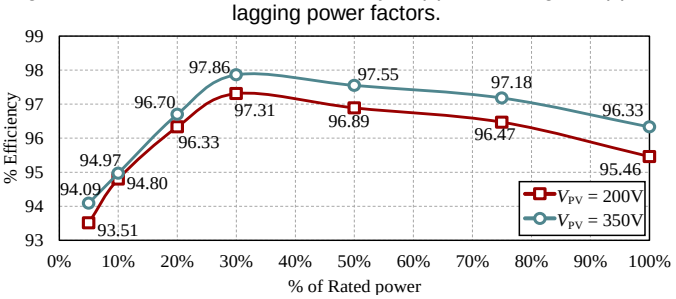

Fig. 22. Efficiency versus output power.

TABLE IV
COMPARISON AMONG FOUR CONFIGURATIONS OF DC SIDE CONVERTER OF DMIMI.

	DCM interleaved	DCM non-interleaved	CCM interleaved	CCM non-interleaved
No. of semiconductors D_{mk} and S_{mk}	4	2	4	2
No. of inductors L_{mk}	2×250 µH	1×250 µH	2×1 mH	1×1 mH
Peak voltage of S_{mk} and D_{mk}	350 V	350 V	350 V	350 V
Peak current of S_{mk}, D_{mk} and L_{mk}	≈11.5 A	≈36 A	≈6.2 A	≈11.5 A
f_{sw}	30 kHz	30 kHz	30 kHz	30 kHz
Peak calculated efficiency of the DMIMI based on Table II	98.41%	98.02%	97.84%	97.32%

V. CONCLUSION

This paper proposes a new dual-mode interleaved multi-level single-phase grid-tied transformerless PV inverter. The operating principles and the converter design guidelines are presented in details. Fast yet simple digital control schemes based on the dead-beat concept are then proposed, which result in excellent DC voltage and AC current control performance. Based on the theoretical analysis and the experimental studies, the proposed converter has the following main advantages:

TABLE V
COMPARISON AMONG THE COMPETITORS.

	IIDMI [10]	Aalborg [11]	Converter in [13]	2-stage DB [14]	Proposed DMIMI
No. of switches	11	6	9	7	10
No. of diodes	3	4	2	5	4
No. of inductors	4	3	2	3	3
No. of capacitors	2	3	2	3	3
No. of DC sources	1	2	1	1	1
No. of semiconductors conducting simultaneously (positive, negative half cycle) during active state mode	3, 3 (interleaved operation)	3, 3	3, 3 @step-down 4, 4 @step-up	3, 3 @step-down 4, 4 @step-up	3, 2 @step-down 4, 4 @step-up (interleaved operation)
No. of semiconductors conducting simultaneously (positive, negative half cycle) during zero state mode	3, 3 (interleaved operation)	3, 3	2, 2	2, 2	2, 1
ZCS operation?	no	no	no	no	yes (step-up stage)
Switching Freq. [kHz]	10	40	20	20	30
Rated power [kW]	2.2	2	0.22	1.5	1
Peak efficiency [%] step-down, step-up modes	98.4, 98.2	98.18, 97.6	96.13, 95.22	97.36, -	97.86, 97.31
Injected current THD [%]	1.9	-	2.9 (5-level) 4.2 (3-level)	-	2.07 (5-level) 2.31 (3-level)
RMS leakage current [mA]	26.8	-	16.2 (5level) 30 (3-level)	12.3	≈20 (5level) ≈5 (3-level)
Low frequency component in current demanded to PV?	yes	yes	yes	yes	yes
Capability of reactive power exchange?	no	no	no	no	yes

1) it retains the advantages of the dual-mode time-sharing inverters as a high conversion efficiency, since only one power stage, either step-down or step-up, works at high frequency at any time, which prevents unnecessary switching losses;

2) although the DMIMI has almost many devices, but it retains the advantages of the single-stage schemes as a decreased number of semiconductors conducting at the same time and better THD of the output current;

3) it retains the benefits of the dead-beat controller as a fast transient response, especially at mode transitions between the step-down and step-up and positive and negative half cycles;

4) it offers a low leakage current;

5) it retains the advantages of the interleaved DC choppers as reduced current through the passive and active components and the increased ripple frequency;

6) it offers reactive power exchange.

The main shortcomings of the DMIMI are the relatively high number of semiconductors (10 switches and 4 diodes) and the presence of high frequency components in V_{CM} during the step-up mode.

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